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FULL IMAGE EXPOSURE OF FIELD WITH ALIGNMENT MARKS

FIELD OF THE INVENTION

001 This invention relates generally to semiconductor processing, and more specifically to the processing of a field of a semiconductor wafer having alignment marks.

BACKGROUND OF THE INVENTION

002 Deposition and patterning are two of the basic steps performed in semiconductor processing. Patterning is also referred to as photolithography, masking, oxide or metal removal, and microlithography. Patterning enables the selective removal of material deposited on a semiconductor substrate, or wafer, as a result of deposition. For example, as shown in FIG. 1A, a layer 104 has been deposited on a substrate 102. After the photolithography process is performed, as shown in FIG. 1B, some parts of the layer 104 have been selectively removed, such that gaps 106a and 106b are present within the layer 104. A photomask, or pattern, is used (not shown in FIG. 1B) so that only the material from the gaps 106a and 106b are removed, and not the other portions of the layer 104. The process of adding layers and removing selective parts of them, in conjunction with other processes, permits the fabrication of semiconductor devices.

003 Alignment is critical in photolithography and deposition, as well as in other semiconductor processes. If layers are not deposited properly, or if they are not selectively removed properly, the resulting semiconductor devices may not function,

relegating them to scrap, which can be costly. Therefore, alignment marks are placed on the semiconductor wafer for the proper positioning during the deposition and photolithography processes. This is shown in FIG. 2, where the semiconductor wafer 202 has alignment marks, such as the alignment square 204, thereon. When the photomask 206 is positioned over the wafer 202, its own alignment marks, such as the alignment square 208, is aligned with the alignment marks of the wafer 202. For example, the alignment square 208 of the photomask 206 is aligned so that the alignment square 204 of the wafer 202 is centered therein.

004 For some types of semiconductor processing, alignment marks are placed in two fields, or areas, on opposite edges of the semiconductor wafer. This is shown in FIG. 3. A semiconductor wafer 300 is divided into a number of fields, such as the field 302. Each field corresponds to one or more semiconductor devices, and represents an area of the semiconductor wafer that will be processed at a given time. For instance, a stepper may first process one field, then move on to the next field, and so on. The wafer 300 has an upper-right field 304 and a lower-left field 306 that have alignment marks 308 and 310, respectively. The presence of the alignment marks 308 and 310 on the fields 304 and 306 presents difficulties with semiconductor processing of these fields, however. In particular, the alignment marks 308 and 310 should not be obscured, as may result from their processing, so that proper alignment for subsequent processing can still occur.

005 A conventional approach to ensure that the alignment marks 308 and 310 are not obscured is to only partially expose the fields 304 and 306 during photolithography, so that the alignment marks 308 and 310 are not exposed. This is shown in FIG. 4. The part

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of the semiconductor wafer 300 is shown that includes the field 304 having the alignment mark 308. The partial-image mask 402 prevents exposure of the part of the field 304 having the alignment mark 308. The mask 402 is positioned over the field 304, as indicated by the dotted line 404, and the field 304 is exposed. The top part of the mask 402 prevents exposure of the top part of the field 304 that has the alignment mark 308. The bottom part of the mask 402 includes a partial image for the field 304, such that the bottom part of the field 304 is exposed. The mask 402 can be a positive photoresist mask. Partial exposure as shown in FIG. 4 may be accomplished by, for example, blade adjustment of the semiconductor equipment being used.

006 The partial exposure process of FIG. 4 has disadvantages, however. The resulting dimensions of the semiconductor device(s) of the field 304 defined by the partial exposure may be inaccurate as compared to the dimensions of the devices defined by the full exposure of other fields. These dimensions resulting from subsequent photolithography, etching, and chemical mechanical polishing (CMP). Furthermore, and possibly also causing the poor dimension uniformity, planarization of the unexposed part of the field 304 having the alignment mark 308 is not uniform to the exposed part of the field 304 and other fields adjacent to the field 304. This is shown in FIG. 5. The area 502 of the field 304 corresponds to the part of the field 304 that was exposed, whereas the area 504 of the field 304 corresponds to the part of the field 304 having the alignment mark 308 (not shown in FIG. 5) and which was not exposed, as divided by the dotted line 506. The area 504 has a greater height than the area 502 does, resulting in a lack of planar uniformity.

007 Therefore, there is a need for exposing the fields of a semiconductor wafer on which there are alignment marks without employing a partial image exposure process. There is a need for such exposure without resulting in poor semiconductor device dimensions. Such exposure should also improve planarization of the parts of the fields having alignment marks, as compared to those parts that do not have alignment marks. For these and other reasons, there is a need for the present invention.

SUMMARY OF THE INVENTION

008 The invention relates to the full image exposure of a field of a semiconductor wafer on which there is an alignment mark. The field of the semiconductor wafer may be located at an edge of the wafer, such as the lower-left or upper-right edge of the wafer, and is exposed using a full-image mask, such as a positive photoresist mask, and that is preferably inclusive of the alignment mark. A clear out process is then performed around the alignment mark on the field of the semiconductor wafer to reveal the alignment mark. Prior deposition of photoresist or other layers, and subsequent exposure and stripping of the photoresist and etching of the other layers may also be performed.

009 The invention provides for advantages over the prior art. Because the entire field is exposed, and not just a part of the field as is done in the conventional partial image exposure process, the semiconductor devices fabricated using the invention have greater planar uniformity as compared to the conventional process. More specifically, there is greater planar uniformity between the part of the field in which the alignment mark is located and the rest of the field. This can result in improved dimensions of the resulting

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semiconductor devices as compared to those when using the conventional process. Still other advantages, embodiments, and aspects of the invention will become apparent by reading the detailed description that follows, and by referencing the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

0010 FIGs. 1A and 1B are diagrams showing the effect of patterning on a layer deposited on a semiconductor wafer.

0011 FIG. 2 is a diagram showing the alignment of a mask to a semiconductor wafer.

0012 FIG. 3 is a diagram of a wafer showing the alignment marks on two fields at the edge of the wafer.

0013 FIG. 4 is a diagram showing the conventional partial image exposure process.

0014 FIG. 5 is a diagram showing the lack of planar uniformity resulting from the conventional partial image exposure process of FIG. 4.

0015 FIG. 6 is a flowchart of a method of an embodiment of the invention.

0016 FIG. 7 is a diagram showing the full image exposure process according to an embodiment of the invention.

0017 FIGs. 8A and 8B are diagrams showing the effects of a clear out process.

0018 FIGs. 9A and 9B are diagrams showing how the clear out process can generally be performed.

0019 FIG. 10 is a diagram showing the clear out process according to an embodiment of the invention.

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0020 FIG. 11 is a diagram showing the improved planar uniformity resulting from the full image exposure process of FIG. 7 and the clear out process of FIG. 10.

DETAILED DESCRIPTION OF THE INVENTION

0021 In the following detailed description of exemplary embodiments of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific exemplary embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized, and logical, mechanical, and other changes may be made without departing from the spirit or scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

0022 FIG. 6 shows a method 600 according to an embodiment of the invention. Not all the parts of the method 600 are necessary to perform the invention, however, nor is the order of the parts illustrated in FIG. 6 the only order in which they can be performed. Other parts and processes may also be performed in addition to or in lieu of those shown in FIG. 6. The method 600 can be used to fabricate a semiconductor device according to an embodiment of the invention.

0023 One or more layers are deposited on the field of a semiconductor wafer having an alignment mark (602). These layers may be silicon layers, metal layers, or other types of layers. The field may be one of the fields 304 and 306 of the wafer 300 of FIG. 3. That

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is, the field may be located at an edge of the wafer, such as the upper-left or lower-right part of the edge of the wafer. Photoresist is next deposited on the field of the semiconductor wafer (604).

0024 The photoresist is exposed using a full-image mask, such as a positive photoresist mask, that is preferably inclusive of the entire field, including the alignment mark on the field (606). A positive photoresist mask is one in which photoresist is subsequently removed from areas that were not protected from exposure by the opaque regions of the mask, but remains after development in regions that were protected from exposure. That is, a positive image of the mask remains following the development process.

0025 FIG. 7 shows an example of this full-image exposure process. The part of the semiconductor wafer 300 is shown that includes the field 304. A full-image mask 702 is positioned over the field 304, as indicated by the dotted line 704, and the field 304 is exposed. The full-image mask 702 corresponds to one or more semiconductor devices for the entire field 304, even the area in which the alignment mark 308 is located. This is as compared to the partial-image mask 402 of FIG. 4, in which there are semiconductor device(s) for only the bottom part of the field 304, and not the top part of the field 304 that includes the alignment mark 308. The entire field 304 is thus exposed in FIG. 7, such that the alignment mark 308 in the field 304 is obscured. The mark 308 may also be obscured because of the previous and/or subsequent deposition of the photoresist and/or the other layers. The alignment mark 308 is thus not depicted in FIG. 7.

0026 Referring back to FIG. 6, the photoresist is developed (608). Development of the photoresist removes the photoresist that was exposed. Those parts of the photoresist that

were not beneath opaque regions of the full-image mask became polymerized, such that development removes them. Conversely, those parts of the photoresists that were beneath opaque regions of the full-image mask remained unpolymerized, such that they remain even after development. The layers previously deposited can then be etched such that they have a pattern substantially identical to that of the full-image mask and the remaining photoresist (610). After etching, the remaining unpolymerized photoresist that was unexposed is stripped to remove this photoresist (612).

0027 Finally, a clear out process is performed to reveal the alignment mark previously obfuscated by the photoresist deposition and exposure processes (614). The clear out process of 614 may also be performed before 608, 610, and/or 612 of the method 600. A general description of the effects of the clear out process is described with reference to FIGs. 8A and 8B. As shown in FIG. 8A, the alignment marks 804 are hidden from view by the photoresist 802 that have been deposited on the silicon wafer, and are indicated as such as dotted. To maintain the alignment marks 804, a photolithographic clear out process is performed, which clears the photoresist 802 from around the alignment marks 804. The results of the clear out process are shown in FIG. 8B, where a window 806 has been created around the alignment marks 304, exposing the underlying silicon wafer.

0028 FIGs. 9A and 9B show how the clear out process can generally be performed. In FIG. 9A, a mask 902 is shown that contains an auxiliary pattern 904. The mask 902 can also be a reticle. The auxiliary pattern 904 contains no device circuitry, and surrounds a smaller pattern 905 in order to clear out a specified window area and isolate the smaller pattern 905. In this case, the auxiliary pattern 904 would correspond to the alignment

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marks 804 of FIG. 8B, such that a part of the photoresist 802 remains surrounded by the alignment marks 804 as shown in FIG. 8B. By comparison, in FIG. 9B, a mask 906 is shown that contains a blank pattern 908, where the mask 906 may also be a reticle. The blank pattern 908 contains no circuitry, and clears out a specified window area, such that no part of the resist 802 of FIG. 8B would remain surrounded by the alignment marks 804 if the blank pattern 908 were used in lieu of the auxiliary pattern 904 of FIG. 9A.

0029 FIG. 10 shows an example of the clear out process as applied to the field 304 of the wafer 300 after the full-image exposure process of FIG. 7 has been performed. A preferably full-image mask 1002 is positioned over the field 304, as indicated by the dotted line 1004. The full-image mask 1002 includes a blank pattern 1006 that corresponds to the area 1008 of the field 304 in which the alignment mark 308 is located. The field 304 is then exposed through the mask 1002. This, optionally in conjunction with a subsequent development process, clears out the photoresist from the area 1008 of the field 304, revealing the alignment mark 308. Revelation of the alignment mark 308 is desired for proper positioning of subsequent etching and deposition processes.

0030 FIG. 11 shows the more uniform planarization that results from the full image and clear out processes of the invention. The area 1102 of the field 304 corresponds to the part of the field 304 that does not include the alignment mark, whereas the area 1104 of the field 304 corresponds to the part of the field 304 having the alignment mark 308 (not shown in FIG. 11). The area 1104 has a height substantially equal to that of the area 1102, meaning that there is greater planar uniformity. This is as compared to the area

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504 of FIG. 5 having a greater height than the area 502 of FIG. 5, resulting from the conventional partial image process and which causes a lack of planar uniformity.

0031 It is noted that, although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and equivalents thereof.

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